Interview Summary	Application No.	Applicant(s)	
	10/550,447	KUBOTA ET AL.	
	Examiner	Art Unit	
	Dieu Hien T. Duong	2821	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Dieu Hien T. Duong*. (3)_____.

(2) *Thomas J. Bean*. (4)_____.

Date of Interview: *05/08/07*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *10*.

Identification of prior art discussed: _____.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

THUY V. TRAN
PRIMARY EXAMINER

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

A teleconference was made to discuss about the corrections to be made to the claims so as to more clearly define the claimed invention and to overcome the teachings of the cited prior art, resulting in an authorized examiner's amendment including:
Claim 10, line 5, insert --, said field effect transistors being complementary;-- after "lamp"; line 11, insert - -, and paired drain terminals for each complementary field effect transistor are arranged side-by-side and project from one side of the package, a gate terminal and source terminal for each complementary field effect transistor are arranged side by side and project from an opposing side of the package- - after "base".